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Power Gating Mechanism Application Wireless Sensor Network Protocol Installation

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Abstract
Wireless sensor networks or Wireless sensors and Actuator networks (WSAN) are spatially distributed autonomous sensors to monitor physical or environmental conditions such as temperature, sound, pressure etc. and to cooperatively pass their data through the network to a main location. In WSN one of the main problem is related to power issue because every node is operated by external battery. To have a large network life time all nodes need to minimize their power consumption. Node is composed of small battery so energy associated with this is very less so replacing or refilling of battery is not possible which is very costly. Today such networks are used in many industrial and consumer applications such as industrial process monitoring and control, machine health monitoring, thermal power plant and so on. This project proposed design for implementation of wireless sensor network protocol for low power consumption by using power gating signal. Power gating technique suggests the implementation of power gates in order to switch off the leakage currents of inactive functional blocks. This technique is primarily seen as a low power option for the emerging multi threshold CMOS (MTCMOS) technology.
Therefore, in this project power gating is consider as the main power saving leverage in wireless sensor nodes and propose novel protocol architecture of the sensor node, which includes a power gating controller and a sophisticated functional-block power gating mechanism.
Keywords: *Wireless sensor network, Power consumption, Power gating, Battery, MTCMOS, Life time of network, Node.*

I. INTRODUCTION

Due to tremendous success of wireless voice and messaging services, it is hardly surprising that wireless communication is beginning to be applied to the domain of personal and business computing. Wireless technology can able to reach virtually every location on the surface of the earth.Wireless sensor network are one of the category belongs to ad-hoc networks. Sensor network are also composed of nodes. Here actually the node has a specific name that is "Sensor" because these nodes are equipped with smart sensors. A sensor node is a device that converts a sensed characteristic like temperature, vibrations, pressure into a form recognize by the users. Wireless sensor networks nodes are less mobile than ad-hoc networks. So mobility in case of ad-hoc is more. In wireless sensor network data are requested depending upon certain physical quantity so wireless sensor network is data centric. A sensor consists of a transducer, an embedded processor, small memory unit and a wireless transceiver and all these devices run on the power supplied by an attached battery. Wireless Sensor Networks (WSNs) refers to highly distributed networks of small and lightweight wireless nodes deployed in large numbers to monitors the environment or system by measuring physical parameters such as temperature, pressure, humidity etc. Each sensor node has a microprocessor and a small amount of memory for signal processing and task scheduling. Each node is equipped one or more sensing devices such as acoustic microphone arrays, video or still cameras, infrared, seismic, or magnetic sensors. Each sensor node communicates wirelessly with a few other local nodes within its radio communication range.

II.PROPOSED METHODOLOGY

Node Level Architecture and Power Consumption

The first step in designing energy-aware sensor systems involves analyzing the power dissipation characteristics of a wireless sensor node. Systematic power analysis of a sensor node is extremely important to identify power bottlenecks in the system, which can then be the target of aggressive optimization. We analyze two popular sensor nodes from a power consumption perspective and discuss how decisions taken during node design can significantly impact the system energy consumption. The system architecture of a canonical wireless sensor node is shown in Figure. The node is comprised of four subsystems:

- Main Controller
- Short Range Radio for Wireless Communication
- A Group of Sensors and Actuators
- A power supply subsystem, which houses the battery and the dc-dc converter, and powers the rest of the node.

Main Controller Unit

Providing intelligence to the sensor node, the main controller unit is responsible for control of the sensors and the execution of communication protocols and signal processing algorithms on the gathered sensor data. The power performance characteristics of main controller have been studied extensively, and several techniques have been proposed to estimate the power consumption of these embedded processors.

Radio

The sensor node's radio enables wireless communication with neighboring nodes and the outside world. Several factors affect the power consumption characteristics of a radio, including the type of modulation scheme used, data rate, transmit power, and the operational duty cycle. In general, radios can operate in four distinct modes of operation: Transmit, Receive, Idle, and Sleep. An important observation in the case of most radios is that operating in Idle mode results in significantly high power consumption, almost equal to the power consumed in the Receive mode. Thus, it is important to completely shut down the radio rather than transitioning to Idle mode when it is not transmitting or receiving data.

Sensors

Sensor transducers translate physical phenomena to electrical signals and can be classified as either analog or digital devices depending on the type of output they produce. There exists a diversity of sensors that measure environmental parameters such as temperature, light intensity, sound, magnetic fields, image, etc. There are several sources of power consumption in a sensor, including signal sampling and conversion of physical signals to electrical ones, signal conditioning and analog-to-digital conversion.

Dynamic Vs Static Power in Sensor Node

The design requirements of a sensor node are typical to all portable and battery powered devices. The main target is to reach maximum performance at minimum power. Since the leakage contribution increases with every new generation of CMOS technology the power optimization has to consider both the static and the dynamic power.

Dynamic Power

The dynamic power is consumed during the active mode of operation. It depends on the supply voltage and applied clock frequency and is linear to the activity factor of a circuit. Reducing one of those parameters will reduce the dynamic power. The common practice to reduce the dynamic power is to apply the clock gating of inactive blocks. Clock gating turns clocks off when they are not needed and thus prevents undesired toggling in the distribution network of the clock.

Static Power

The static power is the power loss due to leakage currents in the circuit. The most important leakage sources are the sub threshold leakage and leakage through the oxide. The latter depends on the oxide thickness and the supply voltage. The more time a circuit spends in idle mode, the higher is the leakage contribution. The straightforward method to reduce the leakage during idle periods is to switch off the idle circuit from the power supply.

III. SYSTEM DESIGN

Back Ground

Battery Issues

The battery supplies power to the complete sensor node and hence plays a vital role in determining sensor node lifetime. Batteries are complex devices whose operation depends on many factors including battery dimensions, type of electrode material used and diffusion rate of the active materials in the electrolyte. In addition, there can be several non idealities that can creep in during battery operation, which adversely affect system lifetime. We describe the various battery non idealities and discuss system level design approaches that can be used to prolong battery lifetime.

Rated Capacity Effect

Every battery has a rated current capacity, specified by the manufacturer. The most important factor that affects battery lifetime is the discharge rate or the amount of current drawn from the battery. Drawing higher current than the rated value leads to a significant reduction in battery life. This is because, if a high current is drawn from the battery, the rate at which active ingredients diffuse through the electrolyte falls behind the rate at which they are consumed at the electrodes.

Relaxation Effect

The effect of high discharge rates can be mitigated to a certain extent through battery relaxation. If the discharge current from the battery is cut off or reduced, the diffusion and transport rate of active materials catches up with the depletion caused by the discharge. This phenomenon is called the relaxation effect and enables the battery to recover a portion of its lost capacity. Battery lifetime can be significantly increased if the system is operated such that the current drawn from the battery is frequently reduced to very low values or is completely shut off. Previously proposed network protocols have often ignored this fact, leading to fallacious

savings in power consumption, as pointed out in. Therefore, the radio should be completely shut off whenever possible to obtain energy savings.

SYSTEM DESIGN

Power Gating Mechanism

Power gating is a design technique used to reduce the overall static power loss of a chip. Compared to the clock gating used to reduce dynamic power, the power gating is more invasive since it affects inter block communication. It adds significant delays and needs a block isolation technique that secures the proper system functionality.

Principles of Power Gating

Power gating may be applied externally (off chip) or internally (on chip). In the first case, a certain block is supplied by a dedicated power supply that can be shut down. In the other, the power switches are implemented on chip. Internal power gating may be a better solution, when there are many blocks to be gated. External gating might be useful to switch off the power of pads. Internal gates are usually distributed around a power-gated block. They create a power gating network that disconnects either Vdd or Vss from the block. The outputs of a power-gated block must be isolated to prevent crowbar currents in an always powered-up block. It is sometimes desirable to retain the internal state of a certain block in power-down mode, and restore this state in power-up mode. The power gating mechanism is controlled by a power gating controller. The controller ensures that each block is properly powered up and down without disturbing the system functionality.

IV. POWER GATED PROTOCOL ARCHITECTURE

Processor

In a power-gated architecture, the processor is active only during the data transmission process, otherwise it sleeps. Its task is to control the communication process and the application. The complete software (firmware) is stored in ROM (e.g. Flash). The firmware may be loaded via debug port or via radio. This protocol processor achieves a higher computational efficiency than the general-purpose microcontroller by exploiting parallelism in the design and implementing protocol specific operations. Consequently, the operating frequency and power consumption can be reduced keeping the same throughput. Main objective is to implement receive and transmit data paths completely in hardware. This is achieved by the CRC components (for frame check sum generation), encryption and decryption blocks, and by direct memory access.

Memory

The memory sub-system consists of program and data memories. The program memory is a flash that shares the same power rail with the processor. The data memory is used to store measured data and for random data access. If the incoming data frequency is low enough, it is possible to use a flash for data storage. The operational RAM is power-gated separately or together with the processor.

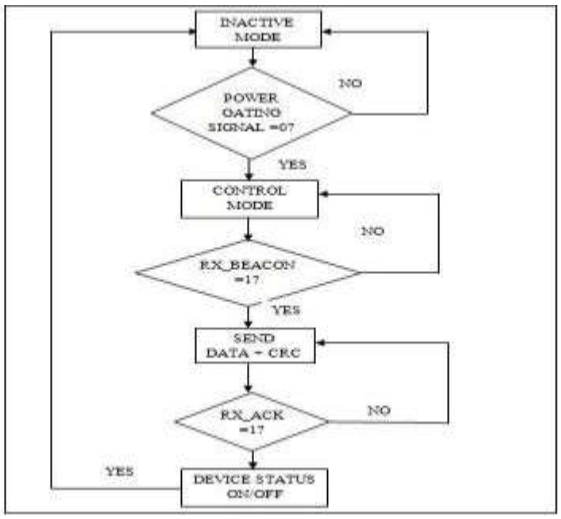
Radio

The radio consumes significant amount of energy whenever transmitting or receiving. Some network protocols use the TDMA-like power management schemes based on wake-up/sleep scheduling to save the power. The wake-up/sleep scheduling approach is not optimal due to a complicated synchronization mechanism that wakes-up the nodes on regular basis. It introduces an overhead because frequently there is no data to transfer but only the synchronization beacons are received. In the case of a sensor node, a solution for this problem can be switching off the node while no activity in the network and switching it on

again when the wake-up event occurs. To support such behavior, one has to implement a low-power radio circuitry that will detect the wake-up signal and initiate the power-up of the node.

Flow Chart for Node Design

In this design we put node in SLEEP Mode (shut down mode) after gating active low POWER GATING signal it will enter in CONTROL mode where it will wait for RX_BEACON signal from receiver. If it get active high signal it will transmit with CRC until it get acknowledgement from receiver depending upon nature of data it will command the device and after getting acknowledgement from receiver it again enter in Inactive mode. The flow diagram for node is shown in fig.

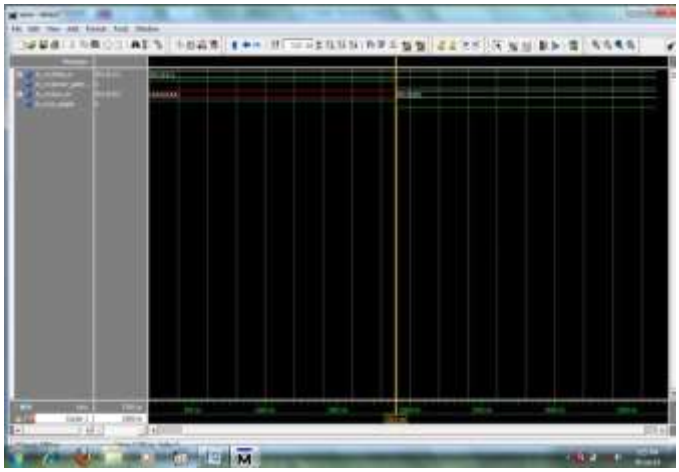


V.SIMULATION AND RESULT

Simulation

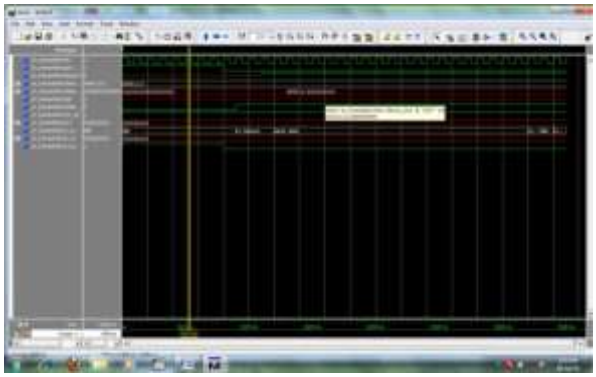
The Simulation is performed on Model Sim SE PLUS 6.3f.The various waveforms has been seen and compared.

Waveform for Cyclic Redundancy Check (CRC)



In above waveform when Power Gating is '1' then output does not occur but when this signal is '0' then output is occurred.

Waveform for Transmitter



In above waveform when Power Gating is disable then transmitter does not transmit data but when Power Gating is enable then it wait for BEACON signal. After receiving BEACON signal it transmit data.

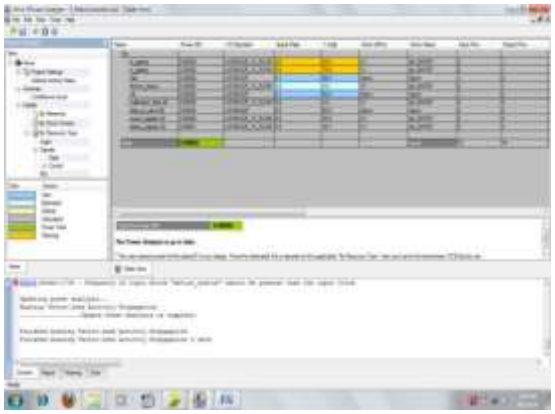
Waveform for Receiver

In above waveform at receiver side, it shows device status '0' before receiving desired data. After receiving desired data it shows device status '1' and send ACK signal to transmitter

Result:

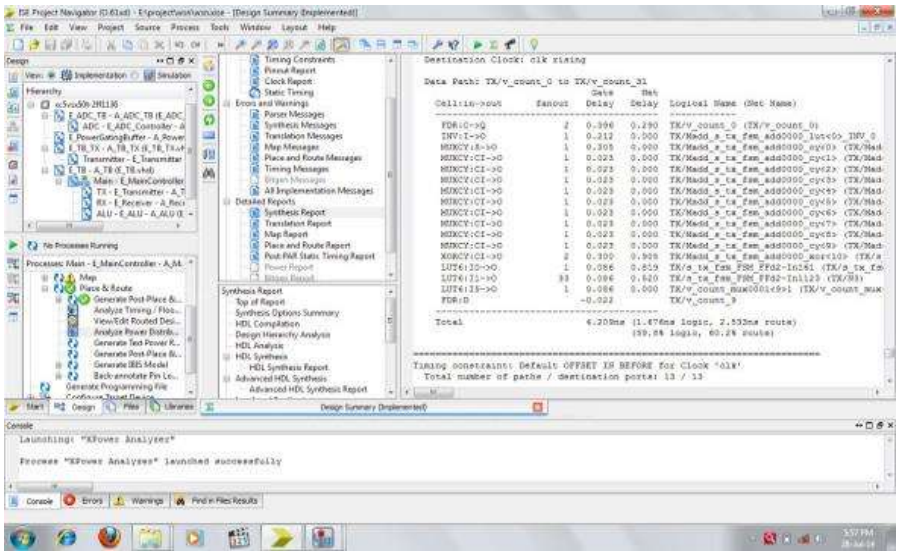
The calculation of total power consumed and calculation of total delay has been performed on Xilinx ISE Design Suit 13.2_1.

Total Power



After implementing all the designed module in Xilinx and by performing power analysis, total power window is available on screen as shown in figure. After giving signal rate of 0.1, the total power can be estimated as **20 µW**.

Total Delay



After implementing all the designed module in Xilinx and by stimulating all codes, detailed synthesis is available. As seen from above window, synthesis report shows total delay of system. i.e. 4.20 ns

VI. CONCLUSION

This project deals with challenges face by wireless sensor network and present design for low power transmitter. Present techniques that are available are complicated and economically costly to implement. The design technique that we have used in this project is robust, low cost and easy to implement. The use of Power Gating signal enables system to meet the low power requirements of wireless sensor node. After implementation and simulation of protocol it is find out that power consume is as low as 20μW so such amount of power saving can lead to significant enhancement in sensor network lifetime. Therefore our approach for implementation of wireless sensor network protocol is simple and cost effective.

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